Thermal Conductivity and Thermal Interface Resistance Measurements of Thin Films using 3ω Method

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ABSTRACT

A large number of experimental and theoretical studies investigating thermal conductivity of both bulk and thin films exist in the literature. For measurement of thermal conductivity of bulk films we have methods like Guarded Hot Plate method, Flash method and for thin films we have methods like Thermo reflectance and Photo acoustic methods. What makes 3ω method different from other methods is that it can be used over a wide range of film thicknesses ranging from nano scale to milli meters. The purpose of the present study is to validate the method and measure thermal conductivity and thermal interface resistance of thin films of varying thickness. In the present study, we have measured thermal conductivity of thin films of SiO_2 of varying thickness deposited on Si substrate and thermal interface resistance of their interfaces. Initially all the required thin films of different thickness were fabricated using different techniques. Firstly, experiments were conducted on a bulk borofloat glass to validate the method, followed by the measurements for thin films. The results are in close accordance with the previous research. The thermal conductivity of borofloat glass was measured to be 1.16 W/mK with a 5.2% deviation from the actual value. In the last section possible sources of error in the final measurements are discussed.

NOMENCLATURE

C	Specific heat Capacity (J/kgK)
$\vec{q}$	Heat flux (W/m^2)
T	Temperature (K)
Ω	Frequency of current source (Hz)
Y	Euler's constant (= 0.577)
P	Electrical resistivity (Ωm)
R	electrical resistance (Ω)
A	thermal diffusivity (m^2/s)
K	thermal conductivity (W/m.k)
L	length of heater line (m)
W	width of the heater line (m)
T	thickness of the heater line (m)
V	Voltage measured (V)
V3ω	Third harmonic of the voltage (V)
I	Current measured (A)
TCR	Temperature coefficient of resistance (/K)
Λ	Thermal penetration depth (m)

1. INTRODUCTION

Nano scale heat transfer is one of the latest research areas that has attracted much attention from researchers all over the world. Study of thermal transport across nanostructures and nano fluids has pushed the frontiers of heat transfer into the nano scale. Study of thermal transport across such nanostructures is different from bulk samples because as the size of a structure decreases, the surface area to volume (S/V) ratio increases and boundary and interface scattering effects dominate over volumetric effects. Hence, nanostructures have a profound impact on the transport of heat and energy by electrons, phonons and photons.

One major driver behind microtechnology and nanotechnology is information processing, which includes microelectronics, data storage, and data transmission. The information carriers are electrons in electrical circuits and photons in optical fibres. The transport of electrons and photons often generate unwanted heat. As more and more devices are compacted into a small area, heat generation density increases and thermal management becomes major challenge for the microelectronics industry.

Low thermal conductivity materials are required to reduce the thermal leakage between the hot and cold sides. The use of nanostructures to control the thermoelectric transport properties for improving the electron energy carrying capability and reducing the thermal conductivity emerged over the last ten years as a very promising approach for realizing highly efficient thermoelectric devices.

An accurate measurement of thermo physical properties of thin films is essential for modeling and predicting thermal performance of such nanostructures and Microsystems. Thermal Conductivity is the most important thermal property of any material and serves as the starting point for any experimental infrastructure.

The thermal conductivity of thin films or other micro and nanostructures can differ from that of bulk samples for several reasons. First, as the size of a structure decreases the surface area to volume ratio increases and boundary and interface scattering effects may dominate over volumetric effects such as umklapp and alloy scattering. Secondly, since thin films are often grown by techniques such as chemical vapor deposition (CVD) or molecular beam epitaxy (MBE) they can contain a microstructure or purity that is different from that of a bulk sample.

Steady state techniques offer the advantage of generally being simple to use, however they have several drawbacks. One such disadvantage is that heat losses due to blackbody radiation can result in a large amount of error. Transient techniques utilize a time-dependent heat flux, typically in the form of a periodic heat source or as a heat pulse, and measure the time dependent temperature change. One significant advantage of transient techniques is that long equilibration times are not needed, as most techniques require only a few periods of heating which generally is on the order of a few seconds.

There are a wide variety of different thermal conductivity measurement techniques for thin films. These techniques were the subject of several comprehensive reviews [1-4] in recent years. However, in recent years the 3ω method has rapidly become one of the most preferred techniques for thin film structures, primary advantage being applicable for a wide range of film thicknesses ranging from bulk to nano scale.

2. BASIC METHODOLOGY

A metal line is evaporated on the thin film whose thermal conductivity is to be measured. The metal line is patterned using standard photolithography techniques. The metal line is used as an electrical resistance heater and temperature sensor, therefore this technique is limited to samples that are electrically insulating (or, more precisely, samples with at least one insulating surface) as any current leakage to the sample will corrupt the measurement. When used for bulk substrates, the heat flow is approximated as radial flow. Current with angular frequency ω is passed through the metal line creating Joule (I^2 R, where I is the current and R is the resistance) heating at 2ω. This heating causes the temperature of the line to also oscillate at 2ω. Since the resistance of a pure metal increases with increasing temperature, the resistance of the metal line also oscillates at 2ω. This 2ω component of the resistance multiplied by the driving current at ω produces a small voltage oscillation at 3ω in the form where $V_3\omega$ is the 3ω component of the voltage.

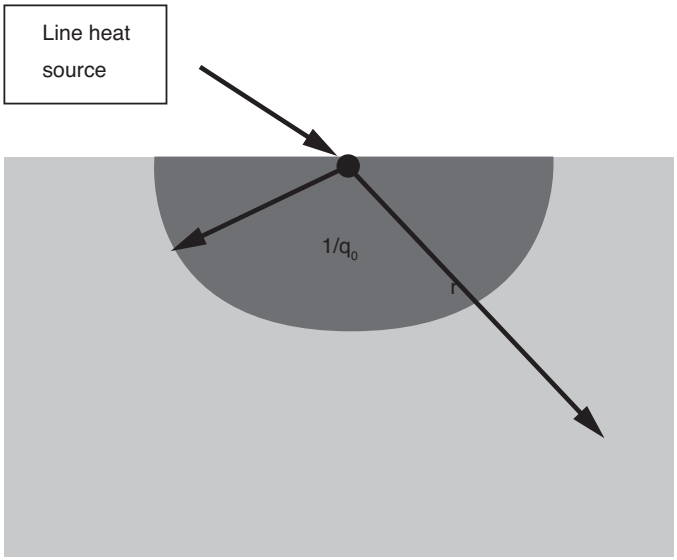

Figure 1. Schematic diagram of line heat source located on the top of solid for thermal conductivity measurement

$$I \sim 1\omega$$
$$T \alpha H \alpha I^2 \sim 2\omega$$
$$R \alpha T \sim 2\omega$$
$$V = IR \sim 3\omega$$

The voltage signal has components of ω and 3ω. The 3ω component is isolated during the measurement. It gives a measure of the temperature oscillations of the surface. When it is plugged into the in-phase component of the equation derived by Cahill (for bulk samples)[10] , it gives thermal conductivity k.

The 3ω technique originally invented by Cahill [7] and now regarded as a standard technique for thermal conductivity measurement on thin film. This method is based on heat diffusion in a semi–infinite solid. A line heat source is located on the top of solid of which you want to measure thermal conductivity. A sinusoidal heat is applied to the line heat source. Thus, the heat affected zone or the thermal penetration depth, 1/q0, depends on the applied heating frequency. In the 3ω method, the heater frequency is set in such a way that the thermal penetration depth is smaller than the size of the solid. In this way, cylindrical heat diffusion equation in semi – infinite solid can be used.

The governing equation of the technique is energy equation in cylindrical coordinates [5].

$$\frac{\partial T(r,t)}{\partial t} = \frac{\alpha}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T(r,t)}{\partial t}\right) \tag{1}$$

where α the thermal diffusivity and T refers to temperature.

In the case of sinusoidal heat source, steady periodic temperature oscillation is assumed to be the solution of the equation (1), which is

$$T(r,t) = T_0 + \Delta T(r)e^{i2\omega t} \tag{2}$$

where ω is circular frequency. T_0 is constant temperature independent of frequency and ΔT is the amplitude of temperature oscillation. If we define the thermal penetration depth as

$$\lambda = \sqrt{\frac{\alpha}{i2\omega}} \tag{3}$$

and substitute (2) in (1), equation (1) can be written as

$$\frac{d^2\Delta T}{dr'^2} + \frac{1}{r'}\frac{d\Delta T}{dr'} - \Delta T = 0 \tag{4}$$

where

$$r' = \left(\frac{i2\omega}{\alpha}\right)^{1/2} \tag{5}$$

Now, the solution of the equation (4) can be found on modified Bessel functions of order υ, which is

$$\frac{d^2y}{dz^2} + \frac{1}{z}\frac{dy}{dz} - \left(1 + \frac{v^2}{z^2}\right) = 0 \tag{6}$$

The boundary conditions used are

$$\Delta T \approx 0 \quad \text{as } r \to \infty \tag{7}$$

$$P = \lim_{r\to 0}\left[-kA\frac{d\Delta T}{dr}\right] = \lim_{r\to 0}\left[-k(\pi rl)\frac{d\Delta T}{dr}\right] \tag{8}$$

where P is the amplitude of power applied to the heat source. Here k is the thermal conductivity of the underlying solid and l is the length of the heat source. The equation (4) can be solved by comparing it with equation (5) and in the limit $\left|\frac{r}{\lambda}\right| \ll 1$, (temperature oscillation at the surface), the amplitude of temperature oscillation at the surface can be approximated as

$$\Delta T(0) = \frac{P}{\pi lk}\left[\frac{1}{2}\ln\left(\frac{\alpha}{r^2}\right) + \ln 2 - \gamma - \frac{1}{2}\ln(2\omega) - \frac{i\pi}{4}\right] \tag{9}$$

where γ = 0.5772(Euler's constant). This is equation (3) in Cahill's paper [7]. The temperature oscillation is composed of real (in-phase oscillation) and imaginary part (out-of-phase oscillation). The real part has dependency over heating frequency but the imaginary part does not.

Extracting thermal conductivity by measuring in-phase temperature oscillation requires at least two different frequencies, just like the following relations.

$$\Delta T(0)_{\omega=\omega_1} - \Delta T(0)_{\omega=\omega_2} = \frac{P}{\pi lk}\left[-\frac{1}{2}\ln\frac{\omega_1}{\omega_2}\right] \tag{10}$$

Therefore, the thermal conductivity of the underlying solid is

$$k = \frac{P}{2\pi l}\frac{\ln\frac{\omega_1}{\omega_2}}{\Delta T(0)_{\omega=\omega_1} - \Delta T(0)_{\omega=\omega_2}} \tag{11}$$

Now, the following equations are derived based on the electrical properties of the heater line.

$$I(t) = I_0 \mathrm{Cos}(\omega t) \tag{12}$$
$$R = R_0(1+\mathrm{TCR}.\Delta T(0)\mathrm{Cos}(2\omega t)) \tag{13}$$

Where I represents the current flowing through the heater, R is the electrical resistance of the heater, TCR is called 'temperature coefficient of resistance' whose definition is given by

$$\mathrm{TCR} = \frac{1}{R}\frac{dR}{dT} \tag{14}$$

Thus the corresponding voltage drop, V across the wire is

$$\begin{aligned} V &= IR \\ &= I_0 \mathrm{Cos}(\omega t).R_0(1+\mathrm{TCR}.\Delta T(0)\ \mathrm{Cos}(2\omega t)) \\ &= I_0 R_0 \mathrm{Cos}(\omega t)+1/2 I_0 R_0.\mathrm{TCR}.\Delta T(0)(\mathrm{Cos}(3\omega t)+\mathrm{Cos}(\omega t)) \end{aligned} \tag{15}$$

As shown in the equation (15), the temperature oscillation on the surface, $\Delta T(0)$, is associated with ω and 3ω components. By measuring the voltage at 3ω, one can extract which is

$$V_{3\omega} = \frac{1}{2} I_0 R_0 \frac{1}{R_0}\frac{dR}{dT}\Delta T(0)$$

$$\Delta T(0) = 2\frac{dT}{dR}\frac{R_0}{V_0}V_{3\omega} \tag{16}$$

which is equation (12) in Cahill's paper [7] (note there is typo in his paper). Now if we put the experimentally determined $\Delta T(0)$ of equation (16) into equation (11), the thermal conductivity of the underlying surface can be determined and the final expression is as follows

$$K = \frac{V^3 \ln\dfrac{\omega_2}{\omega_1}}{4\pi l R^2 (V_{3\omega,1} - V_{3\omega,2})}\frac{dR}{dT} \tag{17}$$

where,

1. V refers to the voltage measured across the heater line
2. ω_1 and ω_2 refer to the frequencies at which the measurements have been made.
3. $V_3\omega$ refers to the voltage measured at the third harmonic, and is referred to as 3ω signal.
4. dR/dT refers to the rate of change of electrical resistance as a function of temperature and comes from the Temp. Coefficient of resistance (Temp.Co) of the heater material.
5. l is the length of the heater line
6. R is the resistance of the heater line

Equation (17) corresponds to equation (13) in Cahill's paper [7]. Deriving this relationship indicates some cautions in using this technique to measure thermal conductivity of underlying solid. Careful selection of heating frequency is essential because the heating frequency should be large enough to have penetration depth large compared with heater width. In this way, the line heat source approximation is valid so the cylindrical heat diffusion equation (1) can be used. Also, the heating frequency should not be that small so that penetration depth should be smaller than the size of underlying solid. In this way, a semi–infinite solid approximation can be used.

2.1. Principle for electrically insulating thin films

Although the 3ω technique was originally designed to measure the thermal conductivity of a bulk underlying solid, it has been extended to measure thermal conductivity of thin film on substrate [8].

In this case, one-dimensional heat conduction through the film is assumed. To satisfy this assumption, there are several requirements. First, the heater width should be wider compared to the thickness of the film, but should be thinner compared to thermal penetration depth for line heat source approximation. Second, the thermal conductivity of the film should be lower than that of the substrate. This can be understood as follows. In the extreme case where the thermal conductivity of the film is the same as the substrate, there will be no temperature drop across the film. In thermal conduction point of view, the film is identical as the substrate. Finally, of course, the heating frequency should be chosen in such a way that thermal penetration depth is a much larger than the thickness of the film.

Under the above assumption, the film thermal conductivity of film can be determined as

$$k_{film} = \frac{P.t}{w.l.\Delta T_{film}} \tag{18}$$

where, P is the power supplied by the heater; w,l,t being the dimensions of the heater and ΔT_{film} is amplitude of the temperature oscillation and is the major parameter of interest. The most important point to be noted is that the measured ΔT is independent of heating frequency and

$$\Delta T_{total} = \Delta T_{film} + \Delta T_{substrate} \tag{19}$$

In the slope method [6], the measured temperature oscillation at the surface, ΔT_{total} from the equation (16), has two contributions. One is from the substrate and the other is from the film as shown in Figure 2. Once the film thickness, film thermal conductivity, heating frequency, heater width, meet the requirements in the previous paragraph, the temperature drop across the film is found to be frequency independent. The temperature oscillation on the substrate is derived based on considering finite width of the heater line. The detailed derivation is available in the literature. The resulting expression is

$$\Delta T_{sub}(0) = \frac{P}{\pi l k_{sub}} \left[\frac{1}{2} \ln \left(\frac{k_{sub}}{C_{sub} (\frac{w}{z})^2} \right) + \eta_{sub} - \frac{1}{2} \ln(2\omega) \right] \tag{20}$$

where w is width of the heater line, and η_{sub} = 0.923. The thermal conductivity of the underlying substrate, k_{sub}, is calculated from the equation (17).

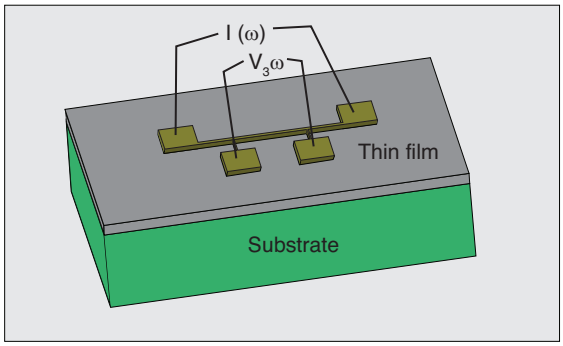

Figure 2. Illustration of 3ω technique for an insulating this film on substrate

2.2. Principle for measuring thermal interface resistance (TIR) of interfaces

Apart from thermal conductivity measurements, 3ω method can be used to find thermal interface resistance of interfaces. In this work, we explored this by fabricating required samples and performing experiments with some calculations as explained in the following.

In order to find TIR of an interface, we need to have two samples fabricated, one with a sandwiched structure over a substrate and another with a film over the substrate.

The temperature difference across both the samples is found out independently using equation (16) and one half of the difference between them gives the temperature difference across the interface, which can be used to find TIR of the interface.

In this work we have fabricated a Cr layer of 10nm thickness sandwiched between two SiO_2 layers of 100 nm thickness over a Si substrate. Also, we have fabricated a Si layer of 10 nm thickness sandwiched between two SiO_2 layers of 100 nm thickness over a Si substrate. The objective is to find TIR of Cr-SiO_2 interface and Si-SiO_2 interface.

One more sample with 200 nm SiO_2 layer deposited on Si substrate is essential to go ahead with the TIR measurement [9].

Considering the Fig.3 and using Cahill's equation (16), temperature difference across the samples can be obtained [3].

$$\Delta T_{total,1} = \Delta T_{SiO2} + \Delta T_{Cr} + \Delta T_{SiO2} + \Delta T_{Si} + 2\Delta T_{Cr\text{-}SiO2}$$

$$\Delta T_{total,2} = 2\Delta T_{SiO2} + \Delta T_{Si}$$

$$\Delta T_{total,1} - \Delta T_{total,2} = \Delta T_{Cr} + 2\Delta T_{Cr\text{-}SiO2}$$

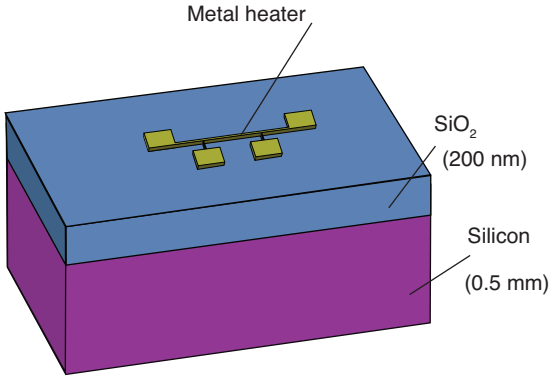

Figure 3. SiO_2 film of 200 nm thickness deposited on Si substrate

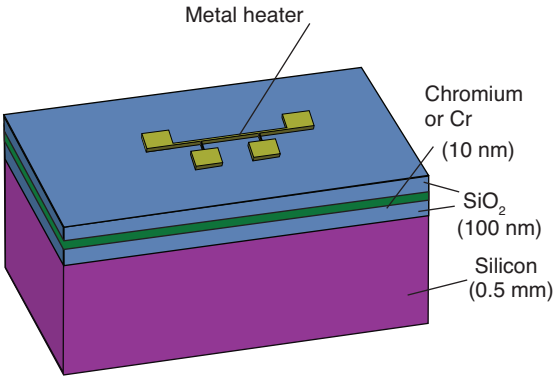

Figure 4. Fabricated Cr sandwiched sample for TIR measurement

Cr is so thin that its thermal resistance is negligible.

$$\Delta T_{\text{Cr-SiO2}} = (\Delta T_{total,1} - \Delta T_{total,2})/2 \tag{21}$$

Using this, the interface thermal resistance can be calculated as follows

$$\Delta T_{interface} = Q_{\text{th}} R_{\text{th}} \tag{22}$$

$$R_{\text{th}} = \frac{\Delta T_{interface}}{Q_{\text{th}}} \tag{23}$$

Here Q_{th} is the heat flux developed due to the resistance of the heater line and Rth is the thermal interface resistance.

3. EXPERIMENTAL DESCRIPTION

This section focuses on design and fabrication of the required samples, with a description of experimental set up.

3.1. Design of metal heater

There are few issues which are to be considered while designing metal heater due to some assumptions and approximations taken. The issues and the corresponding heater design are explained as follows [10]:

3.1.1. One dimensional heat conduction

For the thermal conductivity measurements cross plane, the assumption of one dimensional heat conduction is most essential. For this assumption to be valid,

Heater line width > film thickness

In this work heater line width of 20, 30 and 50microns is designed which is greater than thickness of the films (10nm to 1micron) fabricated.

3.1.2. Line heat source approximation

For this approximation to be valid heater line width should be less than thermal penetration depth through the substrate.

$$\frac{\lambda_s}{b} > 5$$

Here λ_s is thermal penetration depth through the borofloat substrate and b is half of the heater line width.

$$\lambda_s = \sqrt{\frac{D}{\omega}} \tag{24}$$

Here D is thermal diffusivity and ω is heater line frequency. From equation (24) and the condition above it, for a minimum operating frequency of 10.4 Hz, this condition is valid for heater line width of 20, 30 and 50 microns.

3.1.3. Infinite heater length approximation

This assumption is required to neglect end effects.

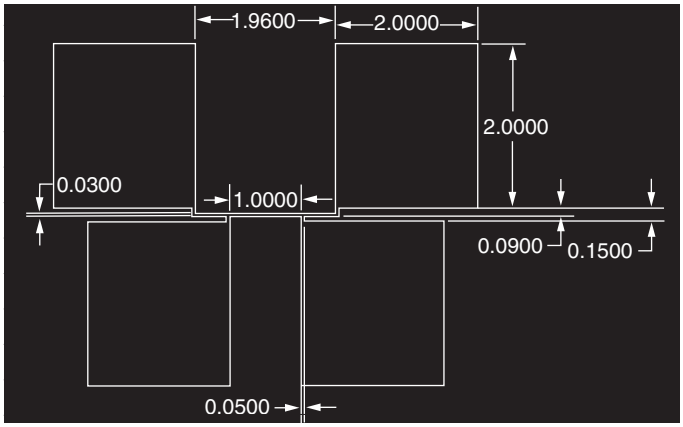

Figure 5. Autocad drawing of a 30micron heater line, displaying the remaining dimensions

$$\frac{L}{\lambda_s} > 4.7$$

For a 1 mm heater line length, minimum operating frequency of 14.46 Hz, this condition is valid.

From 2.1.2 and 2.1.3, heater line frequency > 14.46 will satisfy both the conditions.

The contact pads were given sufficiently large dimension so that wire bonding on them could go on easily.

For practical purposes and to be on safe side, an array of 9 heater lines in a 3 × 3 format is proposed. The three columns have 3 identical heater lines each of a given width. Their widths are 20, 30 and 50 μm respectively. This design using multiple devices is recommended because some of the heater lines may be dysfunctional due to errors in fabrication.

Apart from the earlier discussed approximations and assumptions, there are certain issues which are to be addressed separately for bulk films and thin films.

3.2. Conditions for bulk films

Thermal penetration depth should be large compared with heater width. In this way line heat source approximation is valid.

Thermal penetration depth should be smaller than the size of the underlying solid. In this way, a semi-infinite solid approximation can be used.

$^{*}\lambda_s = \sqrt{\left(\frac{Ds}{\omega}\right)}$, where D_s- thermal diffusivity of substrate and calculated for a frequency of 1500 Hz Here w- heater line width, d_s- thickness of the substrate, λ_s- thermal penetration depth through the substrate.

3.3. Conditions for thin films

Heater width should be greater than film thickness, for one dimensional heat conduction across the film to be satisfied.

Table 1. Approximations to be met for bulk

Approximation	Criteria	On the basis of sample dimensions*
Line heat source	$(\lambda_s /w) > 1$	$(\lambda_s /w) = 1.39$
Semi Infinite solid	$(d_s/\lambda_s) > 1$	$(d_s/\lambda_s) = 23.9$

Table 2. Approximations to be met for thin films. *λ_s and λ are calculated for a frequency of 1500 Hz. #based on the range of film thickness values taken

Approximation	Criteria	On the basis of fabricated sample dimensions*
1D heat conduction	(w/d) > 1	(w/d)= 5000 to 50#
Line heat source	(λ_s /w) > 1	(λ_s /w) = 1.39
Substrate contrast	(k_s/k)>>1	(k_s/k) = 106.43
Penetration through the film	(λ/d) > 1	(λ/d) = 2350 to 23.5#

Heater width should be less than thermal penetration depth, for the line heat source approximation to be satisfied.

Thermal conductivity of the film should be lower than that of substrate.

3.4. Schematic of the experimental set up and working of lock-in amplifier

A Lock-in amplifier is used to detect and measure very small AC signals all the way down to a few nano volts. Accurate measurements may be made even when the small signal is obscured by noise sources many thousands of times larger. Lock-in amplifiers use a technique known as phase-sensitive detection to single out the component of the signal at a specific reference frequency and phase. Noise signals, at frequencies other than the reference frequency, are rejected and do not affect the measurement. The following points have to be kept in mind while operating a lock-in amplifier.

1. A lock-in amplifier always requires a reference frequency to make any measurement. The lock-in only measures the signal at the reference frequency and its harmonics.
2. The value measured is typically the V_{rms} value.
3. Always ensure that the input voltage doesn't exceed 1 volt as a thumb rule for safety of the lock-in amplifier. Never leave open ended cables as stray signals (if stronger) may damage the lock-in amplifier.
4. Measurements made at 50 Hz or its first few harmonics are error prone due to the line frequency (AC power source) being 50 Hz.
5. Use cables ad wires of same length to nullify their effects on measurements.

3.5. Experimental Procedure

The voltage signal from lock-in $V_{sine\text{-}out}$ is connected to one of the contact pad of the sample by BNC cable though one of the terminal, while the other terminal is grounded. Readings from the sample are taken by connecting two BNC cables to two of the contact pads across the heater line. $V_{A\text{-}B}$ option is selected on the panel to get the voltage difference across the heater line, with 'high reserve' on reserve panel.

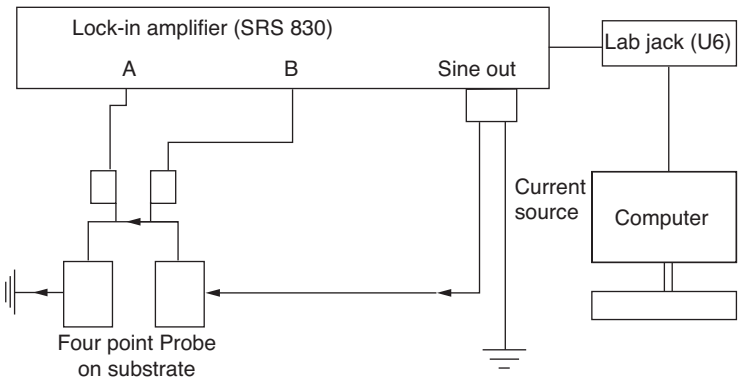

Figure 6. Schematic of experimental set up

However, in this case we need to apply additional correction factor [11] to the equation (16), since our current source is lock-in amplifier, which is not ideal current source, but a voltage source.

$$\Delta T(0) = 2C \frac{dT}{dR} \frac{R_0}{V_0} V_{3\omega} \tag{25}$$

$$C = \left[1 - \frac{R_{line}}{R_{total}} \right]^{-1} \tag{26}$$

$$R_{total} = \frac{V_{sin-out} * R_{line}}{V_{1\omega}} \tag{27}$$

From the above equations the correction factor can be found out.

4. FABRICATION OF THIN FILMS AND HEATER

Based on the metal heater design obtained above, a photomask was developed and all the required SiO_2 films of varying thickness on Si substrate as well as Cr sandwiched and Si sandwiched samples were fabricated in National Nanofabrication Centre, CeNSE, IISc Bangalore.

The fabricated samples were then wire bonded in the Packaging Lab, CeNSE and Centum Electronics Ltd.

4.1. Mask making

A photomask is an opaque plate with holes or transparencies that allow light to shine through in a defined pattern. Photomasks are generally Chrome coated glass lithographic templates designed to optically transfer patterns to wafers or other substrates in order to fabricate planar type devices of all types. This is a pre requisite for any photolithographic process. The mask used is soda lime glass sputtered with chromium.

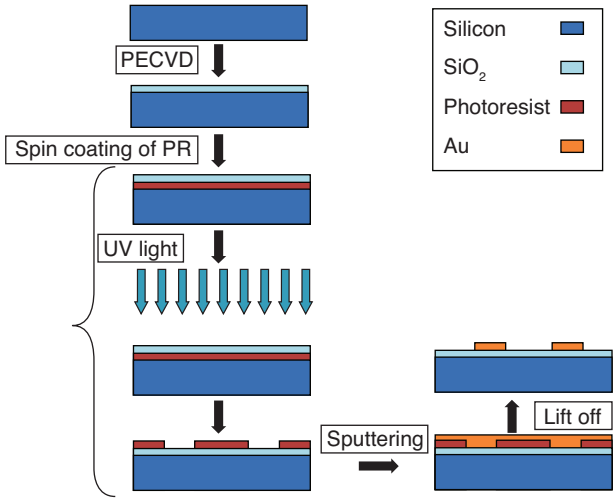

Figure 7. Fabrication process

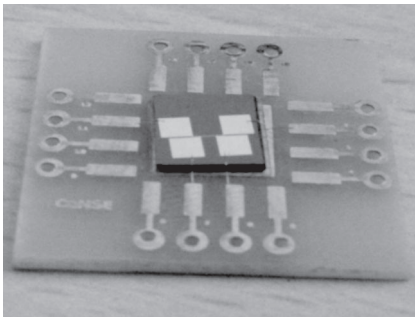

Figure 8. Wire bonding done on a device using Al (33 micron)

4.2. Fabrication of thin films

Two 4inch p-type silicon wafers of 0.5mm thickness were taken, on which SiO_2 layers of varying thickness and Cr sandwiched and Si sandwiched samples were to be developed. The fabrication of the samples involved processes like standard cleaning, and various deposition processes like plasma enhanced chemical vapor deposition (PECVD), thermal oxidation, sputtering etc. and a layer of lithography for metal heater deposition. A typical process flow of majority of the samples fabricated can be seen in Fig. 7.

Following the above process flow, SiO_2 layer of thickness 10 nm, 20 nm, 50 nm, 100 nm, 200 nm, 500 nm and 1000 nm were deposited on Si substrate using PECVD and Thermal Oxidation. Above this layer, a gold layer of thickness 200 nm was deposited using sputtering after lithography and followed by lift off process, to get the required gold pattern on the SiO_2 layer.

Apart from the above samples, two other samples were also fabricated with a 10nm Cr layer and a Si layer sandwiched between two SiO_2 layers, deposited on two different Si substrates, followed by developing the gold pattern on them. These samples were used to find Thermal Interface Resistance between Cr/SiO_2 and Si/SiO_2 interfaces.

Similarly the pattern was developed on a Borofloat glass, which was the starting point of the experiments, since results on this sample were used to validate the set up.

4.3. Wire bonding

In order to interface the metal heater to the measurement circuit contact pads were patterned at both ends of the heater. One way to go for the electrical interface is Wire Bonding.

Packaging and wire-bonding is most widely used method for interfacing microfabricated elements with electronic circuits. It is used where permanent connections are wanted.

A package is a plastic receptacle surrounded by a number of contact pads (thin metal pads, usually made of Gold or Aluminium) linked to metal pins. The chip is bonded to the receptacle and thin wires are bonded between the contact pads on the chip and the package.

The fabricated samples are initially diced to the exact device size with all the four contact pads and metal heater line, using diamond scriber. Since it was a manual process and since we had only 1mm gap between each device on the sample, it was very difficult to dice the sample to the exact device size. And in the process we have lost few devices. So, it is always reliable to go for an automated dicing machine.

The diced samples are then taken for wire bonding and the following steps were followed.

- Silver epoxy and bonding paste were taken in very small quantities and mixed to form a sort of paste. We used this paste to stick our devices onto the PC board.
- The glued devices were then cured in a 80^o C oven for 30 mins.
- Then the samples were taken for wire bonding. Wirebonder is semiautomatic machine to establish connectivity between die and substrate using Au (25 microns), Cu, Al (33 microns) wire using Ultrasonic energy, Force and Time. Ball bonding, Wedge bonding and Ball Bump can be accomplished on this machine. It also has attachments for pick and place, as well as wire pull gauge to test the pull strength. We used Al (33 microns) for few samples and Au (25 micron) for few samples.

The wire bonded devices were then soldered to finish packaging for electrical interface.

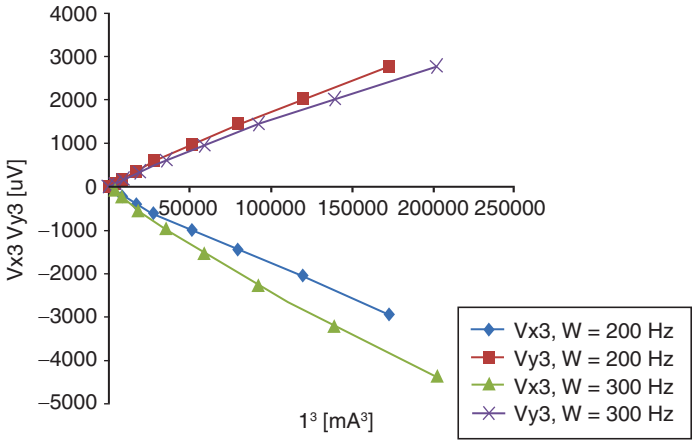

Figure 9. 3ω voltage vs 1ω current, at constant frequency, showing the expected I^3 trend.

5. RESULTS AND DISCUSSIONS

Approaching a 3ω measurement for the first time might be well served by first measuring a thick substrate ($d_s \leq 1$mm) of low thermal conductivity without a film, such as borofloat, to ensure that signals and data processing behave as expected. The advantage of measuring a low k_s substrate is that the signals will be much stronger (see equation (10) [1].

5.1. Validation of experimental set up

Based on 1ω and 3ω electrical transfer functions defined by

$$\frac{V_{\pi\omega,rms}}{2\alpha R_{so}^2 I_{1,rms}^3} = X_n(\omega_1\eta) + jY_n(\omega_1\eta) \tag{28}$$

and for a thermal transfer function Z driven by current I, 3ω voltages should scale with cube of the 1ω current, and the frequency dependence of

$$\frac{V_{3\omega,rms,in\text{-}phase}}{I_{1\omega,rms}^3}$$

should follow the form of –const.+ln(ω) [10], [11].

The bulk borofloat glass, after metal heater fabrication and wire bonding, was connected in an electrical circuit, as shown in the schematic of the experimental set up.

For a fixed frequency of 200 and 300 Hz, by varying the $V_{lock\text{-}in}$, both in-phase and out-of-phase components of V_3, were noted down and plotted against I^3.

For a fixed $V_{lock\text{-}in}$ value of 2V, the $V_3\omega$ in-phase and out-of-phase were noted for a range of frequency and plotted.

From the above performed checks, we can be sure with the experimental set up and go ahead with the thermal conductivity measurements for bulk and thin films.

5.2. Thermal conductivity measurements

5.2.1. Borofloat glass

The borofloat glass was connected in the electrical circuit as shown in the schematic of the experimental setup. It is advisable to perform some basic checks on the lock-in amplifier before

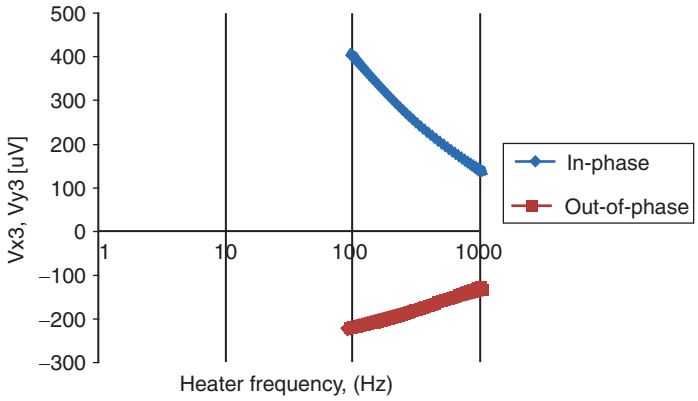

Figure 10. Amplitude of In-phase and Out-of-phase 3rd harmonic voltage oscillations with respect to heater frequency for borofloat glass (500μm) at room temperature

Table 3. Measurements used for calculating thermal conductivity of borofloat glass.

Parameters	**Value (at freq 1)**	**Value (at freq 2)**
$V_{lock\text{-}in}$ in V	2	2
Length (l) in m	0.001	0.001
Frequency in Hz	160	190
Resistance in Ω	8	8
V1ω in V	0.2218	0.2218
V3ω in mV	0.3445	0.322
TCR in /K	0.0014	0.0014
Temperature in K	300	300

Table 4. Measurements taken for a 1000nm SiO_2 film on Si substrate, deposited by PECVD.

Parameters	**Measured Value**
$V_{lock\text{-}in}$ (V)	5
$V_{1\omega}$ (across heater line) (V)	0.4880
R_{line} (Ω)	9.19
R_{total} (across the circuit) (Ω)	94.16
C(correction)=$[1\text{-}R_{line}/R_{total}]^{-1}$	1.108
TCR (K^{-1})	0.0014
Length (m)	0.001
$k_{substrate}$ (W/m.K)	149
C_{sub} (J/kg-K) at 25°C	702.24
Heater line width (μm)	30

heading to the experiment. One basic check could be to connect a BNC cable from $V_{sine\text{-}out}$ to V_A, and check if we are getting the same reading on both the panels. Care has to be taken while performing this check, because sending a voltage value of greater than 1V could be harmful to the lock-in amplifier.

Once the connections are alright, using the equation, and Fig.10, taking differential values from a range, where the 3rd harmonic out-of-phase voltage values are almost constant, the thermal conductivity of borofloat glass, at room temperature is determined to be 1.16 W/m K.

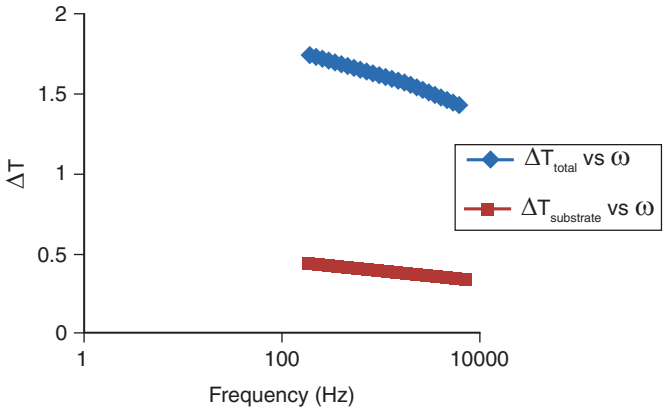

Figure 11. Measured temperature rise on the metal heater/thermometer line for a **1000 nm** SiO_2 film, deposited on a Si substrate by PECVD. ΔT_{film} is found from the relation $\Delta T_{film}=\Delta T_{total}-\Delta T_{sub}$

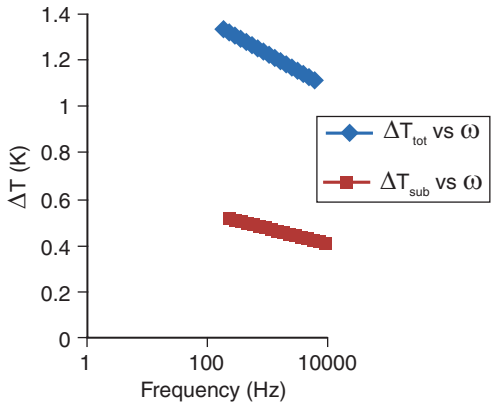

Figure 12. Measured temperature rise on the metal heater/thermometer line for a **500 nm** SiO_2 film, deposited on a Si substrate by PECVD

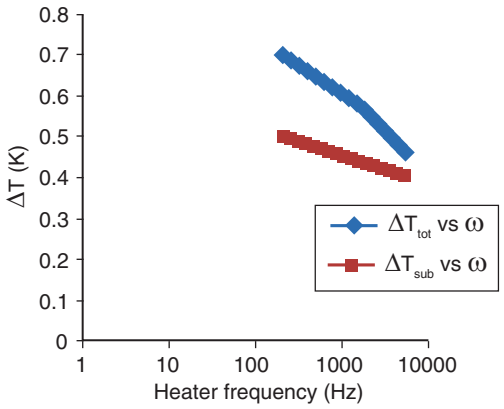

Figure 13. Measured temperature rise on the metal heater/thermometer line for a **100 nm** SiO_2 film, deposited on a Si substrate by PECVD

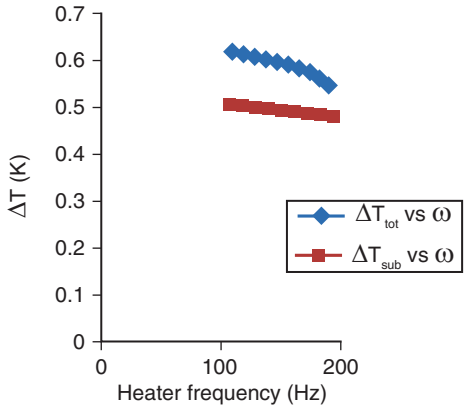

Figure 14. Measured temperature rise on the metal heater/thermometer line for a **50 nm** SiO_2 film, deposited on a Si substrate by PECVD

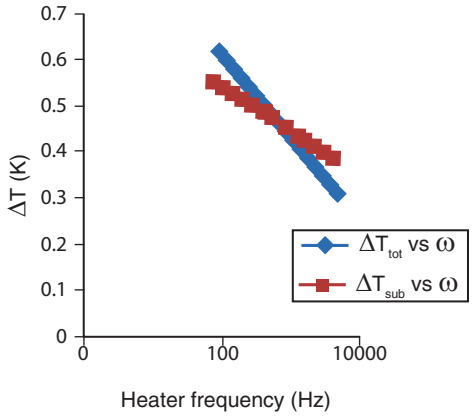

Figure 15. Measured temperature rise on the metal heater/thermometer line for a **20 nm** SiO_2 film, deposited on a Si substrate by PECVD

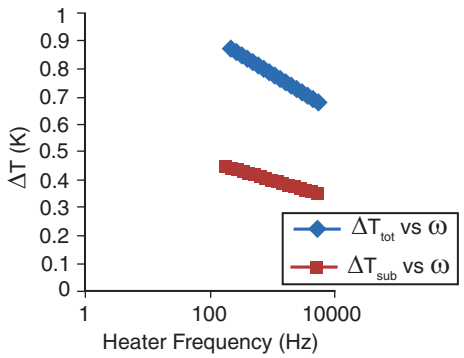

Figure 16. Measured temperature rise on the metal heater/thermometer line for a **500 nm** SiO_2 film, developed on a Si substrate by Thermal Oxidation

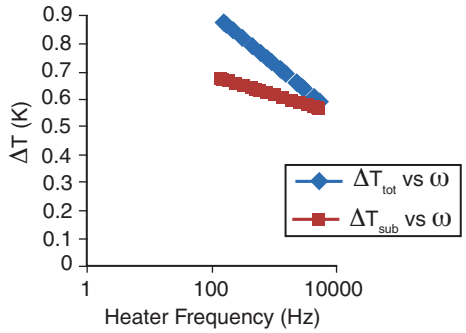

Figure 17. Measured temperature rise on the metal heater/thermometer line for a **100 nm** SiO_2 film, developed on a Si substrate by Thermal Oxidation

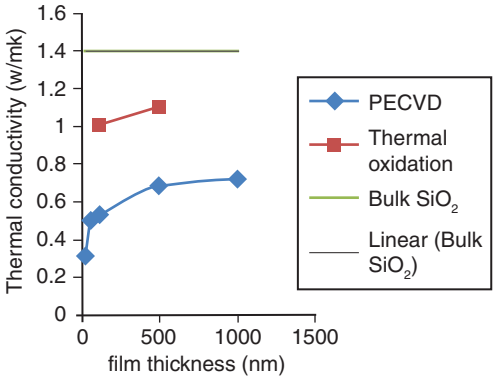

Figure 18. Measured thermal conductivity values of SiO_2 films. A contrast between thermal conductivity values of SiO_2 films developed by different methods can be seen

Ideally the experiments are to be performed in an environmental chamber and put the sample under vacuum conditions to prevent heat transfer to surrounding by convection and radiation. The Temperature Coefficient of Resistance (TCR) value should be calculated based on the electrical resistance values at different temperature, by controlling the temperature of the chamber. Since we had no environmental chamber, we had to go with a literature value of TCR of 0.0014.

5.2.2. Thin films

The wire bonded and soldered samples of SiO_2 film on Si substrate were connected in the circuit and checked with multimeter for any discrepancies in current flow. Thermal conductivity measurements were made on thin films of SiO_2, of varying thickness, deposited on Si substrate of 0.5mm thickness, using the equations (17), (18), (19) and (20).

The measurements and calculations made for a 1000nm SiO_2 film deposited on Si substrate are as follows:

From the ΔT values calculated for the total sample and substrate can be plotted as follows:

Taking ΔT_{film} value from the above and substituting in equation (18), thermal conductivity of 1000nm SiO_2 PECVD if found to be 0.717 W/mK, at room temperature.

A similar approach was followed to get thermal conductivity of other SiO_2 films. The measurements taken for 10nm SiO_2 film and 200nm SiO_2 film came out erroneous, possibly because of minor fabrication defect.

Some of the trends observed are plotted below for different samples.

For the samples, whose ΔT_{total} and ΔT_{sub} trends were not parallel, the thermal conductivity is measured based on the ΔT_{film} value, where ΔT_{total} and ΔT_{sub} are approximately parallel.

The variation in thermal conductivity of SiO_2 films with variation in its thickness and deposition method can be seen in the graph below.

Technique used	3-ω method	C-therm	% Difference
Measured	1.16	1.1	5.2%
Thermal			
Conductivity			

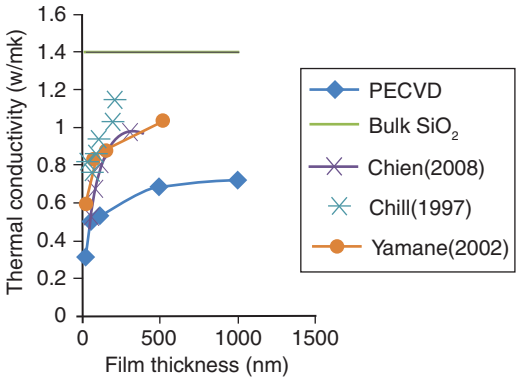

Figure 19. Measured thermal conductivity values of SiO_2 films of varying thickness deposited on Si substrate by PECVD

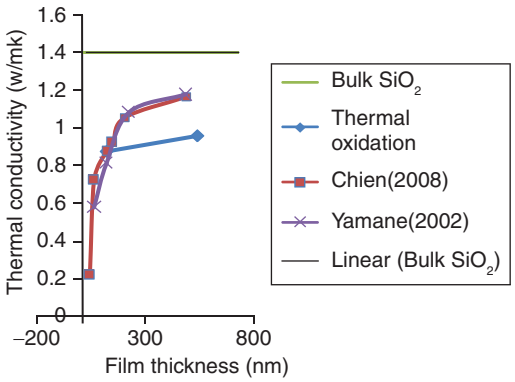

Figure 20. Measured thermal conductivity values of SiO_2 films of varying thickness deposited on Si substrate by thermal oxidation

Table 5. Values used in uncertainty analysis of Borofloat glass

Parameter	Nominal value (u)	Uncertainty(du)	% change (du/u *100)
Length	1000 μm	5 μm	0.5
Resistance	8	0.1 Ω	1.25
TCR	0.0014	0.0001 K^{-1}	7.143
Voltage	221.8 mV	0.1 mV	0.045
$\Delta(V_3\omega)$ signal	322 μV	2 μV	0.621
K	1.16	0.058	5%

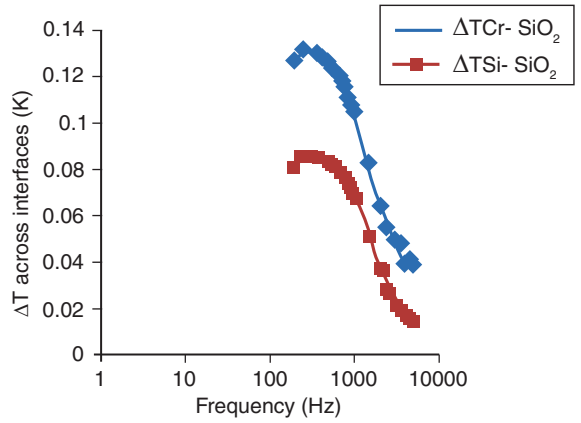

Figure 21. Temperature difference across the interfaces with variation in frequency can be seen

5.3. Validation of result

5.3.1. Borofloat glassThermal conductivity of Borofloat glass was measured by C-therm instrument to be 1.1 W/mK.

5.3.2. Thin films

On comparing our experimental data of thermal conductivity measurement to the previous experimental data [10], we get the following trend for SiO_2 films of varying thickness deposited on Si substrate.

5.4. Uncertainty analysis

Any experimental method is not complete without uncertainty analysis. There are several possible sources of error or uncertainty in the measurements. The variables with uncertainty in the thermal conductivity measurements of the thin films are the length, width, resistance, and *TCR* of the heater line, the heating voltage, the thickness of the film, and 3ω voltage across the line. There are uncertainties in each of these parameters, which propagate through the calculation resulting in an overall uncertainty in the measured thermal conductivity of the film. One common method used to estimate the uncertainty of a result was the following. If the final result (y) is a is a function of several measured variables (x1, x2, , xn) each with a corresponding uncertainty (u1, u2, , u3), the overall uncertainty (uy) from the method of Kline and McClintock[12] is calculated using the following equation.

$$u_y = \left[\left(\frac{dy}{dx_1} u_1 \right)^2 + \left(\frac{dy}{dx_2} u_2 \right)^2 + \cdots + \left(\frac{dy}{dx_n} u_n \right)^2 \right]^{1/2}$$

5.4.1. Uncertainty analysis for borofloat glass

The above table lists the independent parameters used in the measurement of thermal conductivity and sample values of these parameters at a particular frequency. The uncertainty in k is calculated based on the above table.

5.5. Thermal interface resistance

Firstly, a sandwiched structure, an ultrathin Cr layer of 10 nm sandwiched between two 100 nm thickness PECVD SiO_2 layers, deposited on Si substrate, is taken and ΔT across it is found out. By subtracting ΔT across a 200 nm SiO_2 film, deposited on a Si substrate, from the previous value and dividing the result by 2, ΔT across Cr-SiO_2 interface can be obtained as explained in equations (21), (22) and (23) [10]. Similarly TIR of Si-SiO_2 interface can also be obtained.

TIR of Cr-SiO_2 interface and Si-SiO_2 interface were obtained to be 3.73218E-08 and 2.13084E-08 respectively.

6. CONCLUSION

The results and corresponding validation of the results, suggest that we have successfully established the set up for measurement of thermal conductivity of thin films using 3ω method for room temperature.

The basic objectives of this project are thus accomplished.

- Thin films of SiO_2 of varying thickness on Si substrate, Cr layer sandwiched between SiO_2 films as well as Si layer sandwiched between SiO_2 films on Si substrate and metal heater on top of SiO_2 film are fabricated.
- The experimental set up is validated by measuring thermal conductivity of a bulk substrate (borofloat glass).
- Thermal conductivity of a thin film (SiO_2 film on Si substrate) was measured using 3ω method and the trend in variation of thermal conductivity of SiO_2 films with variation in film thickness and method of fabrication was observed.
- Thermal interface resistance of Si-SiO_2 interface and Cr-SiO_2 interface was measured.

From the uncertainty analysis, it can be inferred that the major sources of uncertainty are the $V_3\omega$ signal and the measured resistance of the heater film. To reduce the uncertainty in measurement of resistance it is suggested that a more accurate potentiometer be used in the experiment.

To decrease the uncertainty in the $V_3\omega$ signal, its value has to be increased. This can be achieved by increasing the current signal, which in turn can be achieved by decreasing the ballast resistance or by using a stand alone current source.

In our experimental set up, we have used maximum $V_{sine\text{-}out}$ voltage to achieve the same.

The following are some of the issues in general, which need to be dealt with to get better outcome.

6.1. Ambient temperature

The experiments were performed at room temperature, in open. There might be temperature fluctuations due to opening and closing of the nearby door or due to localized heat sources like laptops. Hence, it is suggested to do the experiments in an environmental chamber and use vacuum to avoid heat loss due to convection and radiation. Also by using an environmental chamber the thermal conductivity can be found out at different temperatures, increasing the versatility of the experimental set up.

6.2. Use of the TCR value from literature

Ideally, the TCR of gold deposited on each sample has to be found out individually, by using an environmental chamber to control the temperature and note the change in electrical resistance of the heater line with variations in temperature.

6.3. Disturbances in using Lock-in Amplifier

The lock-in amplifier is a very sensitive instrument and the measurement of weak signals is prone to disturbances. The presence of computers and a lan router in the vicinity added to the disturbances. Also any mechanical disturbances in the cables/wires leads to stray signals corrupting the measurements. These issues need to be looked into for more accurate measurements. Sometimes the values can be misleading although they follow required trend due to disturbances in BNC cables.

6.4. Dicing the fabricated samples

Dicing of the samples could be very tedious and tough if sufficient gap is not provided between each device on the sample. The gap could be more then 2mm. It is advisable to be aware of this problem while drawing the metal heater pattern for mask making.

7. ACKNOWLEDGEMENTS

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